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# Hamid Shojaei

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## Education

- **2001 - 2003**
- M.Sc. – Computer Architecture
- ECE Department – Faculty of Engineering –University of Tehran – Tehran/Iran(<http://www.ut.ac.ir/>)
- GPA: 17.8 of 20
- Research area: Formal Verification
- Thesis: Coverage metrics in Formal Verification
- Thesis grade: 20 of 20
- Advisor: Professor Zainalabedin Navabi
  
- **1997 – 2001**
- B.Sc. – Computer Engineering
- Isfahan University of Technology – Isfahan/Iran(<http://www.iut.ac.ir/>)
- GPA: 15.43 of 20.0 (Ranked 3st among Hardware Engineering Students in that year)
- Thesis : “Design and implementation of an microcontroller based roll caller”
- Advisor: Professor Pejman Khadivi

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## Awards

- Best Paper Award, 13th Iranian Conference on Electrical Engineering (ICEE 2005), Hamedan, Iran, May, 2005
- Ranked 50th among more than 5,000 applicants in the nationwide graduate examination, Tehran/Iran 2002
- Ranked 3st among hardware engineering students of Isfahan University of Technology, Tehran/Iran 2000.
- Ranked 1st in province in high-school graduation exams, Isfahan/Iran, 1997 (Graduated with GPA: 19.89 of 20)

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## Research Interests

- CAD tool developing such as verification and synthesis using C, C++.
  - Compiler Programming using lex , yacc and ParGen.
  - Digital System Design using VHDL , Verilog
  - Hardware and specification languages
  - Boolean Circuit Complexity and Decision Diagrams
  - Verification coverage analysis
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**Publications****Book:**

- [1] **Hamid Shojaei**, Zainalabedin Navabi, "VLSI Hand Book, Chapter 92: Verification Languages", VLSI Handbook, Second Edition, CRC press, 2006.
- [2] **Hamid Shojaei**, " A Guide to Master Test of Computer Engineering" , Text book, Pardazesh Publisher, 2004.
- [3] **Hamid Shojaei**, " LabVIEW Programming Language: Instrument controlling and automation " ,Text Book, Naghoos publisher 2003.

**Paper:**

- [1] **Hamid Shojaei** , Majid Nabi, Siamak Mohammadi, Zainalabedin Navabi, " A practical approach to assignment coverage estimation in formal verification", to be appeared in 16th Asian Test Symposium (ATS'07), October 9-11, Beijing, China, 2007.
  - [2] Mohammad Rezae Kakoe, **Hamid Shojaei**, Marjan Sirjani, Zainalabedin Navabi, "A New Approach for Design and Verification of Transaction Level Models" IEEE International Symposium on Circuits and Systems (ISCAS 2007), May 27-30<sup>th</sup> , New Orleans, USA, 2007.
  - [3] **Hamid Shojaei**, Mohammad Rezae Kakoe, " Signal Coverage Computation in Formal Verification", 14th Annual IEEE, IFIP International Conference On Very Large Scale Integration (VLSI-SOC 2006), October 16-18th, Nice, France, 2006.
  - [4] **Hamid Shojaei**, Mahmood Askari, "Novel Approach to Signal Coverage Computation in Formal Verification of Hardware Systems", Proceedings of The XXI Conference on Design of Circuits and Integrated Systems(DCIS 2006), November 22-24<sup>th</sup>, Barcelona, Spain,2006.
  - [5] **Hamid Shojaei**, Habib Ghayumi, "Techniques for Formal Verification of Digital Systems: A System Approach", proceedings of Euromicro Symposium on Digital System Design (DSD 2004), August 31 - September 3, Rennes, France, 2004.
  - [6] Pejman Lotfi, Mohammad Hosseinabady, **Hamid Shojaei**, Mehran Massoumi, and Zainalabedin Navabi, "TED+: A Data Structure for Microprocessor Verification", Proceedings of ASP-DAC 2005, Shanghai, China, January, 2005.
  - [7] Pejman Lotfi, **Hamid Shojaei**, and Zainalabedin Navabi, "Property Intermediate Representation with Extensibility", Proceedings of Latin American Test Workshop ( LATW 2004), Cartagena, Colombia,2004.
  - [8] Pejman Lotfi, **Hamid Shojaei**, Hadi Parandeh-Afshar, Zainalabedin Navabi "Improving Logic-Level Representation of BMD/TED Diagrams", Proceeding of 13th Iranian Conference on Electrical Engineering (ICEE 2005), Hamedan, Iran, May, 2005. **[BEST PAPER AWARD]**
  - [9] **Hamid Shojaei**, Hadi Parandeh Afshar, Zainalabedin Navabi,"VHDL Based Symbolic Model Checker with Improved CTL Property Language", Proceeding of International Computer Conference (CSICC 2004), Tehran, Iran, February, 2004.
  - [10]Hadi Parandeh, **Hamid Shojaei**, Zainalabedin Navabi,"A new method for FSM testing(simulation replacement)", Proceeding of International Symposium on Telecommunication (IST 2003), Iran, 2003.
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**Research  
Experience**

**Fall 2002-present: Researcher and CAD Tool Developer**  
**CAD Group, ECE Department, Faculty of Engineering, University of Tehran,**  
**Iran.**

- Research and development of CAD Tools for Verification.
- Research and development of CAD Tools for Synthesis.
- Developing efficient data structures for PSL representation
- Developing Lookup table based technology mapping.
- Contribution in developing VHDL Compiler using Lex and Yacc and generate parse tree.
- Contribution in extracting Data Flow Graph from VHDL description.
- Extracting BDD form VHDL code using CUDD package.
- Converting VHDL to BLIFMV for using in VIS package.
- Contribution in developing a TED (Taylor Expansion Diagram) data structure for using in high level formal verification and generating it from VHDL description.
- Developing a Symbolic Model Checker using TED data structure.
- Developing a Dynamic Model Checker Based on BDD.
- Contribution in High level formal verification using integer equations.
- Developing theorem proving techniques for design verification.
- Developing automatic test pattern generation techniques using DFG.
- Adding some new features to VIS such as
  - Ability for accepting primary inputs in CTL formula as precondition.
  - Accepting VHDL by converting it to BLIFMV
  - Enhancements in engine.
  - Working on using software formal verification methods in hardware verification.

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**Teaching  
Experience**

**2003-present**

- **Faculty member**, Azad University of Damavand, Tehran, Iran(<http://www.damavandiau.ac.ir>)
  - C++ programming( 2003-present)
  - Data Structure(2004)
  - Digital logic Design(2003 – present)
  - Principle of Networks ( 2004)
  - Numerical Computation (2006)
  - Microprocessors(2006)

**Fall 2002:**

- **Instructor** in ITRC Training Center
  - AVR Microcontroller

**2003 – 2005:**

- **Teaching assistant** in Electrical and computer engineering Department, University of Tehran, Tehran, Iran
    - Undergraduate Course of “Digital logic circuits”  
Instructor: Prof. Zainalabedin Navabi
  - **Teaching assistant** in Electrical and computer engineering Department, University of Tehran, Tehran, Iran
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- graduate Course of “Formal Verification”  
Instructor: Dr. Bijan Alizadeh

**Fall 2004:**

- **Teaching Assistant**, Electrical Department, Sharif University, Tehran, Iran
  - Undergraduate Course of “Digital logic circuits”  
Instructor: Dr. Bijan Alizadeh
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**1998-1999:**

- **Teaching assistant** in Electrical and computer engineering Department, Isfahan University of Technology, Isfahan, Iran
    - Undergraduate Course of “Computer Graphic”  
Instructor: Dr. Maziar Palhang
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**Work  
experience**

**2004-present:**

- **NovinFarnoud, an EDA Company** (<http://www.novinfarnoud.com>)
  - Manager of all Projects
  - Developer of Model Checking Engine
  - Executive Manager of HDL Analyzers
  - Developer of Property analyzer

**2002 – 2004:**

- **CADLAB, University of Tehran** (<http://cad.ece.ut.ac.ir>)
  - Leader of verification project
  - CAD Tool Developing Expert Specially in Formal Verification and coverage analyzer

**2001-2002:**

- **Iran Telecommunication Research Center(ITRC)** (<http://www.itrc.ir>)
- **Technical Support Manager and Senior Consultant**
  - Major projects:
    - Synchronous Digital Hierarchy (SDH)
      - FPGA Implementation of HDLC protocol
      - Implementation of ethernet protocol
      - Design and implementation of an microcontroller based roll caller

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<b>Computer Skills</b>	<ul style="list-style-type: none"><li>▪ Programming languages:<ul style="list-style-type: none"><li>• HTML, C++, Visual C++, Pascal, 8086,8051 Assembly, LabVIEW</li></ul></li><li>▪ Hardware Programming:<ul style="list-style-type: none"><li>• VHDL, Verilog, SystemC.</li></ul></li><li>▪ CAD Tools:<ul style="list-style-type: none"><li>• Modelsim, Leonardo, Maxplus, Quartus.</li></ul></li><li>▪ Operating systems:<ul style="list-style-type: none"><li>• Unix, Linux, Windows.</li></ul></li><li>▪ Microsoft Tools:<ul style="list-style-type: none"><li>• Office Tools, Visio.</li></ul></li><li>▪ Others:<ul style="list-style-type: none"><li>• MATLAB</li></ul></li></ul>
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<b>Presentation</b>	<ul style="list-style-type: none"><li>▪ Hamid Shojaei, Masoumeh sayyaran, “ Signal Coverage Computation in Formal Verification”, 14th Annual IEEE, IFIP International Conference On Very Large Scale Integration (VLSI-SOC 2006), October 16-18th, Nice, France, 2006.</li><li>▪ Hamid Shojaei, Habib Ghayumi, “Techniques for Formal Verification of Digital Systems: A System Approach”, proceedings of Euromicro Symposium on Digital System Design (DSD 2004), August 31 - September 3, Rennes, France, 2004.</li><li>▪ Hamid Shojai, Hadi Parandeh Afshar, Zainalabedin Navabi,“VHDL Based Symbolic Model Checker with Improved CTL Property Language”, Proceeding of International CSI3 Computer Conference (CSICC 2004), Tehran, Iran, February, 2004.</li><li>▪ Hadi Parandeh, Hamid Shojai, Zainalabedin Navabi,“A new method for FSM testing(simulation replacement)”, Proceeding of International Symposium on Telecommunication (IST 2003), Iran, 2003.</li><li>▪ Hamid Shojai, Zainalabedin Navabi,“A new coverage metric in symbolic model checking”, 2nd National Computer Conference (2ncc 2003) 10-12 December, Mashhad, Iran, 2003.</li></ul>
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<b>Languages</b>	Farsi,English( PBT Toefl 570)
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<b>References</b>	Available on request
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